REMARKS

As noted previously, the Applicant appreciates the Examiner's thorough examination of the subject application.

Claims 1-29 are pending in the subject application. All of claims 1-29 were rejected in the final Office Action of 14 October 2008 on various grounds, as described in further detail below. No claims are amended herein and no new matter has been added.

Reconsideration and further examination of the subject application is respectfully requested in view of the following remarks.

Claim Rejections – 35 U.S.C. § 102

Concerning item 5 of the Office Action, claims 1-3, 7-10, 12, 14, 16-19, 21, 23, 25-26, and 29 were rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent No. 6,725,357 to Cousin ("Cousin"). Applicant traverses the rejection and requests reconsideration for the following reasons.

For a rejection under 35 U.S.C. § 102(e), the cited reference must teach each and every limitation as arranged in the claim(s) at issue. The independent claims of the subject application recite, *inter alia*, that the instruction packet defines at least two control instructions (claims 1, 26) or comprises two or more control instructions (claim 29). In this situation, **Cousin fails to teach each and every limitation of independent claims 1, 26, and 29**, as will be explained.

Claim 1 (representative of the independent claims under rejection) recites the following:

> A computer processor, the processor comprising:
> (a) a decode unit for decoding a stream of instruction packets from a memory, each instruction packet comprising a plurality of instructions;
> (b) a first processing channel comprising a plurality of functional units and operable to perform control processing operations;
> (c) a second processing channel comprising a plurality of functional units and operable to perform data processing operations;
> wherein the decode unit is operable to receive an instruction packet and to detect if **the instruction packet defines (i) at least two control instructions or (ii) a plurality of instructions one or more of which is a**

> **data processing instruction**, and wherein when the decode unit detects that **the instruction packet comprises at least two control instructions said control instructions are supplied to the first processing channel for execution in program order**.
>
> [Emphasis Added]

In contrast, Cousin fails to teach at least a decode unit detecting "**if the instruction packet define (i) at least two control instructions**".

While the Examiner cites, in the Response to Arguments section of the Office Action, a portion of Cousin (col. 4, lines 41-46) as teaching an instruction word that is 128-bits in length, which are said to be equivalent in some cases to 8 16-bit instructions, the Examiner's conclusion that these instruction would necessarily include more than one control instruction is erroneous, as will be explained.

It is clear from figure 2 of Cousin and column 4, lines 32-36 of Cousin ("*According to a second instruction mode, two instructions each having a length of 32 bits are supplied to the decoder...for example W0 and W1 in the cycle 0...*") that in GP32 instruction mode a pair of instructions is passed to the decoder each cycle. This pair of instructions comprises two 32 bit instructions W0 and W1, or W2 and W3, which are decoded by the decoder 8 and sent to the relevant slots (Slot0 or Slot 1). Figure 2 of Cousin also makes it clear that Instruction0 and Instruction1 (W0 and W1) are to be executed together in the same cycle Cycle 0, and Instruction2 and Instruction3 (W2 and W3) are to be executed together in the following cycle Cycle 1. It is not possible, for example, for an Instruction1 and an Instruction2 to be processed together as they are from different instruction pairs executed in different cycles. **Only one of the two 32 bit instructions W0 and W1, or W2 and W3 (Instruction0 and Instruction1, or Instruction2 and Instruction3) can be a control instruction for the general unit**. This is apparent when looking at the further steps of the Cousin process as explained below.

The two 32 bit instructions Instruction0 and Instruction1 are then processed by the micro instruction generator 10. The Instruction0 in Slot0 can give rise to a micro-instruction in either or both of the two micro-slots labeled μSlot0, and the Instruction1 in Slot1 can give rise to a micro-instruction in either or both of the two micro-slots labeled μSlot1. The micro-instructions

are then sent from the μSlot0 or μSlot1 to a data unit DU1, DU0, an address unit AU1, AU0 or a general unit (a control processing unit).

As stated above, a "macro-instruction" is not directed to the general unit, a macro-instruction (being either of the pairs of 32-bit instructions in a 128-bit GP32 Instruction Word) is decoded by the decoder 8 and then processed by the micro instruction generator 10. **It is a micro-instruction which is directed to the general unit.**

Furthermore, Cousin teaches at column 6, lines 32 to 34 that "**The instructions in the first and second arrays will not both be for the general unit at the same time**" and at column 7, lines 4 to 6 that "**In embodiments of the invention, instructions for the general unit are not provided in both slots at the same time**". It is not possible for the left-hand pair of μSlots to contain instructions for the address unit or the general unit. The right-hand pair of μSlots may be used to supply instructions to the address units and the general unit. However, it is not possible for both the right-hand μSlots to contain instructions for the general unit as stated explicitly at column 6, lines 32 to 34 and column 7, lines 4 to 6 of Cousin.

Since, Cousin teaches that it is not possible for both the right-hand μSlots to contain instructions for the general unit, it is not possible for the two Slots (Slot1 and Slot0, between the Decoder 8 and μInstruction Generator 10 of Cousin Figure 1) to both contain Instructions destined for the General Unit. This is evident from Cousin's description of the function of the μInstruction Generator 10 and its place in the pipeline (3.32 *et seq*, 4.16 *et seq*), which makes clear that the contents of μSlot0 must come from Slot0 and the contents of μSlot1 must come from Slot1, and that Slot0 and Slot1 are processed in the same cycle (illustrated in Figure 2 of Cousin).

Therefore, since it is not possible for both the Slots to contain instructions for the general unit at the same time, **it is not possible for any pair of 32-bit instructions passed to the decoder to comprise only instructions for the general unit (only control instructions)**, in complete contrast with the recited limitations of independent claims 1, 26, and 29. Therefore in the processor disclosed by Cousin, instruction pairs such as (W1,W0) in Cousin's Figure. 2 cannot contain Control Instructions (destined for the General Unit) in both Instruction0 (W0) and

Instruction1 (W1) positions, or likewise in both Instruction2 (W2) and Instruction3 (W3) positions. Cousin teaches that the GP16 and VLIW modes have similar restrictions.

Hence, Cousin does not disclose a decode unit detecting "**if the instruction packet define (i) at least two control instructions**" as claimed in the independent claims of the subject application, since Cousin explicitly states that "***instructions for the general unit are not provided in both slots at the same time***" and consequently, a GP32 Instruction pair would not comprise instructions only for the general unit.

Because of at least the foregoing reasons, Applicant respectfully submits that Cousin is an improper basis for a rejection of claims 1-3, 7-10, 12, 14, 16-19, 21, 23, 25-26, and 29 under 35 U.S.C. § 102(e), and the rejection should be removed accordingly.

Claim Rejections – 35 U.S.C. § 103

Claims 4-5, and 11

Concerning item 6 of the Office Action, claims 4-5 and 11 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Cousin, previously cited, in view of U.S. Patent No. 6,880,150 to Takayama ("Takayama"). Applicant traverses the rejection and requests reconsideration for the following reasons.

One requirement necessary for a rejection under 35 U.S.C. § 103(a) is that the cited reference(s) teach or suggest all of the limitations in the claim(s) at issue. In this situation, Takayama is not understood as teaching the deficiencies (noted previously) of Cousin relative to independent claim 1 (the base claim for claims 4-5 and 11). Because of at least the foregoing reason, Applicant respectfully submits that the combination of Cousin and Takayama is an improper basis for a rejection of claims 4-5 and 11 under 35 U.S.C. § 103(a), and accordingly requests withdrawal of the rejection.

Claims 6, 22, and 24

Concerning item 7 of the Office Action, claims 6, 22, and 24 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Cousin, previously cited. Applicant traverses the rejection and

requests reconsideration for the following reasons.

One requirement necessary for a rejection under 35 U.S.C. § 103(a) is that the cited reference(s) teach or suggest all of the limitations in the claim(s) at issue. As was previously described, Cousin fails to teach or suggest the limitations of claim 1 (the base claim for claims 6, 22, and 24). Because of at least the foregoing reason, Applicant respectfully submits that Cousin is an improper basis for a rejection of claims 6, 22, and 24 under 35 U.S.C. § 103(a), and accordingly requests withdrawal of the rejection.

Claims 13 and 15

Concerning item 8 of the Office Action, claims 13 and 15 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Cousin, previously cited, in view of U.S. Patent No. 5,956,518 to DeHon ("DeHon"). Applicant traverses the rejection and requests reconsideration for the following reasons.

One requirement necessary for a rejection under 35 U.S.C. § 103(a) is that the cited reference(s) teach or suggest all of the limitations in the claim(s) at issue. In this situation, DeHon is not understood as teaching the deficiencies (noted previously) of Cousin relative to independent claim 1 (the base claim for claims 13 and 15). Because of at least the foregoing reason, Applicant respectfully submits that the combination of Cousin and DeHon is an improper basis for a rejection of claims 13 and 15 under 35 U.S.C. § 103(a), and accordingly requests withdrawal of the rejection.

Claim 20

Concerning item 9 of the Office Action, claim 20 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Cousin, previously cited, in view of "Variable Length Instruction Compression for Area Minimization", Piia Simonen, Ikka Saastamoinen, Jari Nurmi, 2003, IEEE ("Simonen"). Applicant traverses the rejection and requests reconsideration for the following reasons.

One requirement necessary for a rejection under 35 U.S.C. § 103(a) is that the cited reference(s) teach or suggest all of the limitations in the claim(s) at issue. In this situation, Simonen is not understood as teaching the deficiencies (noted previously) of Cousin relative to independent claim 1 (the base claim of claim 20). Because of at least the foregoing reason, Applicant respectfully submits that the combination of Cousin and Simonen is an improper basis for a rejection of claim 20 under 35 U.S.C. § 103(a), and accordingly requests withdrawal of the rejection.

Claims 27 and 28

Concerning item 10 of the Office Action, claims 27 and 28 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Cousin, previously cited, in view of Andrew S. Tanenbaum; Structured Computer Organization, 1984; Pg. 10-11 ("Tanenbaum"). Applicant traverses the rejection and requests reconsideration for the following reasons.

One requirement necessary for a rejection under 35 U.S.C. § 103(a) is that the cited reference(s) teach or suggest all of the limitations in the claim(s) at issue. In this situation, Tanenbaum is not understood as teaching the deficiencies (noted previously) of Cousin relative to independent claim 26 (the base claim for claims 27 and 28). Because of at least the foregoing reason, Applicant respectfully submits that the combination of Cousin and Tanenbaum is an improper basis for a rejection of claims 27 and 28 under 35 U.S.C. § 103(a), and accordingly requests withdrawal of the rejection.

Conclusion

For the foregoing reasons, Applicants submit that all of the claims under consideration in the subject application are in condition for allowance. A timely Notice of Allowance for the application is therefore earnestly solicited.

Should the Examiner have any questions, he is invited to call the undersigned.

Authorization is hereby given to charge our deposit account no. 50-1133 for a Petition for Extension of Time (three months) under 37 CFR § 1.136 and for any other fees that may be required for the prosecution of the subject application.

Respectfully submitted,

McDERMOTT WILL & EMERY LLP

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/G. Matt McCloskey/

G. Matthew McCloskey, Reg. No. 47,025
Attorney for Applicants
28 State Street
Boston, MA 02109-1775
Telephone: (617) 535-4000
Facsimile: (617)535-3800